Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **NULL**
2. **– IN**
3. **+ IN**
4. **– VS**
5. **CCOMP**
6. **OUTPUT**
7. **+ VS**
8. **NULL**

**.067”**

**.054”**

**1 8 7**

**6**

**5**

**4**

**2**

**3**

**MASK**

**REF**

**829**

**A**

**D**

**I**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 829**

**APPROVED BY: DK DIE SIZE .054” X .067” DATE: 2/11/16**

**MFG: ANALOG DEVICES THICKNESS .018” P/N: AD829S**

**DG 10.1.2**

#### Rev B, 7/19/02